REMARKS

Claims 56-58, 71, and 72 are pending in the application with claim 56 amended herein, new claims 71 and 72 added herein, and claims 40-55 and 70 canceled herein. Claims 1-39 and 59-69 were previously canceled.

Applicant previously filed a Supplemental IDS on November 9, 2005 listing an English translation of Toru (JP 06-097300) relied upon by the Office. Subsequently, at the Applicant's request, the translator reviewed the translation for clarity and grammar. A re-translation was performed upon finding that the first translation lacked clarity and contained numerous grammatical errors. Applicant respectfully requests that the Office replace the first translation with the second translation that accompanies this Response to November 22, 2005 Office Action.

Claims 40-47, 56-58, and 70 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Without admitting to the propriety of the rejection, Applicant herein amends claim 56, addressing, among other things, the alleged lack of written description. Applicant requests withdrawal of the written description rejection in the next Office Action.

Claims 56-58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Toru (JP 06-097300) in view of Miyanaga (5,418,187). Applicant requests reconsideration.

Amended claim 56 sets forth integrated circuitry that includes, among other features, a series of first conductive polysilicon lines directly on and in contact with a BPSG layer and electrically insulative oxide material on and in

contact with respective first series conductive lines. A top of the insulative oxide material defines a first plane. A plurality of insulative oxide sidewall spacer pairs are on respective sidewall pairs of individual first series conductive lines. Respective spacer tops are coplanar with the first plane and are connected with the electrically insulative oxide material. Individual first series conductive lines are effectively insulated by the BPSG layer, the respective sidewall spacer pairs, and the respective insulative oxide material. The integrated circuitry includes a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with said first plane. The series of second conductive lines are directly on and in contact with the BPSG layer and the first series conductive lines provide cross-talk shielding for the second series conductive lines.

Pages 9-11 of the Office Action allege that Toru discloses every limitation of claim 56 except for the BPSG layer and relies upon Miyanaga to remedy such deficiency. Applicant traverses on the grounds that Toru fails to disclose or suggest the second plane defined by the second series conductive lines being coplanar with the first plane defined by the first series conductive lines. In addition, Applicant herein amends claim 56 to include further limitations not alleged in the Office Action as disclosed in Toru or Miyanaga, considered alone or in combination.

Page 10 of the Office Action alleges that the edge of Toru's conductive layer 11 in contact with "the top part" of insulative film 4 discloses the planes of both materials as being coplanar. Applicant notes that previous and

current claim 56 set forth that the top of the insulative oxide material defines the first plane and that the line tops of the second series conductive lines defines the second plane. The top of insulative film 4 is clearly shown in Toru Fig. 1 at a particular elevational level. The top of conductive layer 11 is also clearly shown in Toru Fig. 1 at a particular elevational level different from the elevational level for insulative film 4. No part of conductive layer 11 reaches the elevational level of the top of insulative film 4. It is thus irrelevant whether conductive layer 11 contacts a "top part" of insulative film 4 since the elevational levels for such materials do not coincide.

Applicant herein establishes adequate reasons supporting patentability of claims 56-58, 71, and 72 and requests allowance of all pending claims in the next Office Action.

Respectfully submitted,

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(54) [Title of invention]
A structure between the wiring of integrated semiconductor circuits

(57) [Abstract]
[Purpose]
This purpose of this invention is to create a structure between the wiring of an integrated semiconductor

circuit that suppresses interference between the wiring, even when the space between the wiring is very small.

[Construction]
This invention makes use of a conductive wired layer (11), which has no effect on the operation of the circuit elements, and is placed in between each wire (1) on the surface of the integrated semiconductor circuit between the insulating films (4 and 5). The conductive layer (11) works as a buffer between the wiring (1) by preventing the transmission of noise from one wire to the other, and thus reducing interference between the wiring.

[Key to the figure]
1. Lower layer wiring (wiring)
2. Upper layer wiring
3. Interlayer insulation film (insulation film)
4. Interlayer insulation film (insulation film)
5. Conductive layer

[Scope of claims]
[Claim 1] A structure between the wiring of an integrated semiconductor circuit that features a conductive layer (which does not affect the operation of the circuit elements) placed in the insulating film between the wiring on the surface of the integrated semiconductor circuit.
[Claim 2] A structure between the wiring of an integrated semiconductor circuit that features a conductive layer inserted into the insulating film between the upper and lower wiring layers, in such a way that it separates the upper and lower wiring layers and does not affect the operation of the circuit elements.

[Detailed explanation of the invention]
[0001]
[Field of industrial application]
This invention relates to the wiring structure of integrated semiconductor circuits.

[0002]
[Conventional technology]
Existing integrated circuit technology consists of circuit elements such as transistors, capacitors, and resistors made from conductive materials such as aluminum, or other kinds of wiring. An insulating film usually separates the wiring electrically; however, as the degree of integration increases the distance between wiring gets smaller, and a 2nd and 3rd layer of wiring is usually added using an interlayer film.

[0003]

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Figure 3 shows a cross-section view of the wiring structure of a conventional integrated circuit. In this figure, (1) is a lower layer of wiring where several wires lay parallel on the same surface; (2) is an upper layer of wiring above the lower layer wiring (1) and arranged so that several wires lay in a perpendicular direction to the lower layer of wiring (1). (3) is a base insulating film covering the bottom surface of the lower layer wiring (1). (4) is an insulating film covering the side and top surfaces of the lower layer wiring (1). (5) is a base insulating film covering the bottom surface of the upper layer wiring (2), and placed between the insulating film (4) and the upper layer wiring (2); and (6) is an insulating film covering the side and top surfaces of the upper layer wiring (2).

[0004]
Therefore, the lower (1) and upper (2) wiring layers have perfect electrical separation from each other by virtue of the insulating films (3 ~ 6), and each layer can send electric signals independently to their respective interlocked circuit elements. If this is to be a digital signal, it is a high/low pattern signal that switches between 0V ("low status") and several Volts ("high status") in intervals ranging from nanoseconds to microseconds. Therefore, the lower (1) and upper (2) layers of wiring are required to send an electric signal to target circuit element in accurate and rapid manner.

[0005]
[Problems to be resolved by the invention]
However, as the degree of integration has increased in these circuits to the extent that an upper (2) and lower (1) layer of wiring is used as outlined above, the distance between the wiring both within a layer and between layers has become very small. Therefore, interference among the wiring occurs more easily within the same layer, and between the lower (1) and upper (2) layers of wiring.

[0006]
In other words, if noise arises for some reason in one wire, this noise is easily transferred to nearby wiring nearby (both above/below or right/left), which results in electric signals not being transmitted to the respective circuit elements in an accurate and fast manner.

[0007] This invention is designed to solve the above-mentioned problem by providing a structure between the wiring of an integrated circuit that significantly reduces interference between the wiring, even when the distance between the wiring is very small.

[0008]
[Steps in solving the problem]
The first step of this invention is to have a conductive layer that does not affect the operation of the circuit elements placed in the insulating film between the wiring, and on the same layer as the wiring, of the integrated semiconductor circuit.

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[0009]
The second step of this invention is to have a conductive layer that does not affect the operation of the circuit elements placed in such a way as to separate the lower layer wiring and upper layer wiring in the insulating film between the lower and upper layers of wiring in the integrated semiconductor circuit.

[0010]
[Operation of the invention]
To accomplish the first step of this invention, it is necessary to have a conductive layer that does not affect the operation of the circuit elements placed in such a way as to separate the lower layer wiring and upper layer wiring in the insulating film between lower and upper layer wiring of the integrated circuit, so that this conductive film layer acts as a buffer between lower and upper layer wiring, and prevents the transfer of noise to other nearby wires when noise occurs in one of the wires. In other words, it prevents interference between nearby wires.

[0011]
To accomplish the second step of this invention, it is necessary to have a conductive layer that does not affect the operation of the circuit elements placed in such a way as to separate the lower layer wiring and upper layer wiring in the insulating film between the lower and upper layers of wiring in the integrated so that if noise occurs in any of the wires, the conductive layer will act as a buffer between the lower and upper levels of wiring to prevent the transmission of noise between the layers. In other words, it prevents interference between the lower and upper layers of wiring.

[0012]
[Working example]
A working example of this invention is described below and makes use of a diagram.
Example 1: Figure 1 shows a working example of a structure between the wiring of an integrated circuit to accomplish step one of this invention. The numbers for the different elements in this diagram correspond to the same numbers as explained for figure (3) previously.

[0013]
In this figure, (11) is a multi-conductive layer that does not affect the operation of the circuit elements (i.e. no electric signal is applied), and is designed to be mounted in the concave space between the interlayer film (4) and the lower layer wiring (1). This material is formed by CVD (Chemical Vapor Deposition) with polysilicon doped with an impurity such as W (tungsten), P (phosphorus), or B (boron). In addition, interlayer insulating film (5) is formed on top of this conductive layer (11).

[0014]

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An explanation of the operation of this conductive layer (11) follows:

The conductive layer (11) is a conductive material placed parallel to the lower layer wiring (1) on the same surface as the wiring in such a way that is blocks out the spaces between the lower layer wires so that it acts as a buffer (impingement protection) between the wires in the lower layer and prevents interference between the lower layer wires. Therefore, if noise occurs for any reason in any one of the lower layer wires (1), the noise will be absorbed by the conductive layer (11) bordering the lower layer wire (1), and this conductive layer will prevent the transfer of noise to any other lower layer wire (1). This conductive layer (11) can be placed in the same fashion between the upper layer wires (2).

[0015]
Maintaining the electric potential of this conductive layer (11) in between the high-low digital signal patterns that occur throughout the lower layer wiring (1) prevents delay or deterioration of the electric signal caused by capacity coupling between the wires when both low and high signals exist simultaneously between nearby lower layer wires (1).

[0016]
In other words, the interlayer insulating film (4) is dielectric, and in order to create a capacity (inter-wire capacity) between nearby wires in the lower layer of wiring (1), an electric signal must progress through the lower layer wiring (1) while the capacity is charged. Therefore, if a low signal and a high signal arise simultaneously in two nearby wires, a large inter-wire capacity develops, causing a delay or deterioration of the electric signal, which can further result in a slower access time (operation speed) or even in malfunction. In this case, the conductive layer (11) maintains an electric-potential somewhere in between the high and low signals, thus holding the capacity between the wires to a small value. As a result, delay of electric signal or deterioration of electric-potential will not occur and the electric signal will be transferred to the circuit elements accurately and rapidly.

[0017]
In addition, since the conductive layer (11) is applied to the concave space between the lower layer wires (1) and the interlayer insulating film (4), the structural level difference is reduced, making the manufacturing process simple, and improving the reliability of the element.

[0018]
Example 2: Figure 2 shows a working example of a structure between the wiring of an integrated semiconductor circuit to accomplish the second step of this invention. (12) is a flat, thin conductive film formed on the interlayer insulating film (4) and does not affect the operation of circuit elements. It uses the same material and is formed using the same method as in Example 1 for the conductive layer (11). Also, the other structures, such as the wiring of the integrated circuit, are the same as in Example 1.

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[0019]
The conductive film (12) is placed to separate the lower layer wiring (1) and the upper layer wiring (2). It acts as buffer between these layers. In addition, a portion of the conductive film (12) between lower layer wires (1) is placed crookedly in the concave portion of the interlayer film (4) so that it comes between lower layer wires (1) and acts as buffer between the lower layer wires (1).

[0020]
Therefore, when noise occurs in any one of the lower layer wires (1), the conductive film (12) prevents noise transfer to nearby lower layer wires (1), while also preventing the transfer of noise to the upper layer wiring (2) nearby. In addition, if noise occurs in any of the upper layer wiring (2), the conductive film (12) prevents the transfer of noise to the lower layer wiring (1).

[0021]
This conductive film (12) can maintain a middle value of electric-potential between high/low signals to prevent delay of electric signal or deterioration of electric-potential caused by capacity coupling between wires when both low and high signal exists simultaneously between nearby wires.

[0022]
In the above-mentioned Example 2, the lower layer wiring (1) of the conductive film (12) is also placed crookedly in the concave spaces between the individual lower layer wires (1). However, it could also be placed crookedly in the concave spaces between the upper layer wires (2). In this case, if noise occurs any one of the upper layer wires (2), the conductive film (12) can prevent noise transfer to nearby upper layer wires (2) as well as noise transfer to the nearby lower layer wiring (1).

[0023]
[Effect of the invention] When this invention is applied as described above, the following effects can be observed:

[0024]
According to the first step of this invention, a conductive layer that does not affect the operation of the circuit elements is placed in the insulating film between wires on the same layer of the integrated circuit. This conductive layer acts as a buffer, which can adequately control wire interference between the wires even if the distance between the wires is very small.

[0025]
According to the second step of this invention, a conductive layer that does not affect the operation of the circuit elements is placed in such a way as to separate the lower layer wiring from upper layer wiring in the

insulating film between lower and upper layers of wiring in the integrated semiconductor circuit. This conductive layer also acts as buffer, which can adequately control wire interference between the lower and upper layers even if the distance between these layers is very small.

[Brief description of the drawings]
[Figure 1] A frame format cross-section diagram of the wiring structure of an integrated circuit relating to Example 1 of this invention.
[Figure 2] A frame format cross-section diagram of the wiring structure of an integrated circuit relating to example 2 of this invention.
[Figure 3] A frame format cross-section diagram of the wiring structure of a conventional integrated circuit.

[Legend]
1. Lower layer wiring (wiring)
2. Upper layer wiring (wiring)
4. Interlayer insulating film (insulating film)
5. Interlayer insulating film (insulating film)
11. Conductive layer
12. Conductive layer film

[Figure 1]
1. Lower layer wiring (wiring)
2. Upper layer wiring
4. Interlayer insulating film (insulating film)
5. Interlayer insulating film (insulating film)
11. Conductive layer

[Figure 2]
12. Conductive layer film